

# IR2153/IR2153D

## SELF-OSCILLATING HALF-BRIDGE DRIVER

### Features

- Floating channel designed for bootstrap operation Fully operational to +600V Tolerant to negative transient voltage dV/dt immune
- Undervoltage lockout
- Programmable oscillator frequency

$$f = \frac{1}{1.4 \times (R_T + 75\Omega) \times C_T}$$

- Matched propagation delay for both channels
- Micropower supply startup current of 90  $\mu$ A.
- Shutdown function turns off both channels
- Low side output in phase with  $R_T$
- IR2153D has built in bootstrap diode

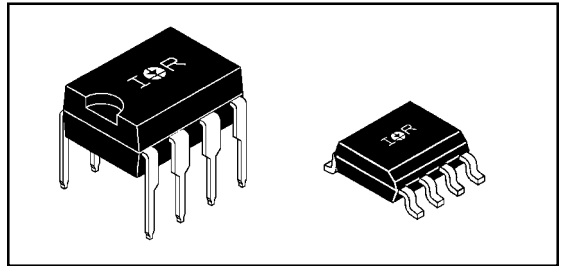
### Description

The IR2153/IR2153D is a high voltage, high speed, self-oscillating power MOSFET and IGBT driver with both high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The front end features a programmable oscillator which is similar to the 555 timer. The output drivers feature a high pulse current buffer stage and an internal deadtime designed for minimum driver cross-conduction. Propagation delays for the two channels are

### Product Summary

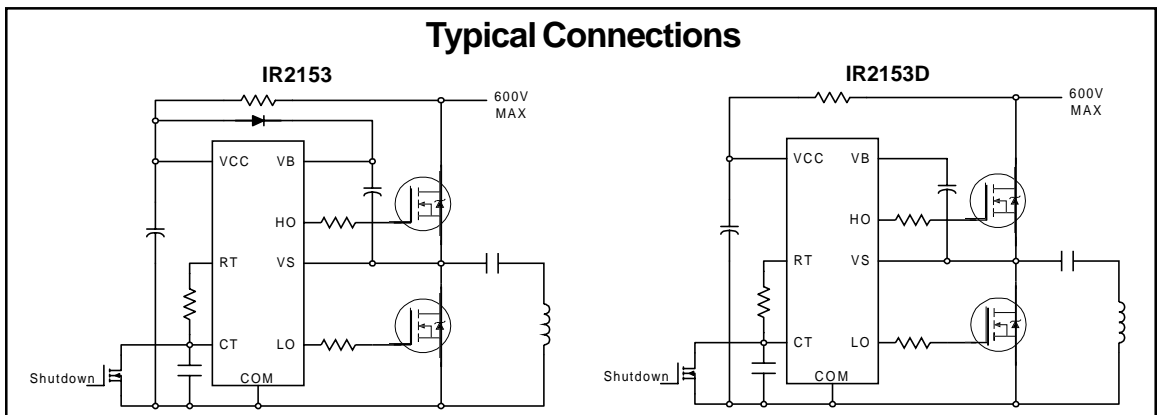
<b>V<sub>OFFSET</sub></b>	<b>600V max.</b>
<b>Duty Cycle</b>	<b>50%</b>
<b>I<sub>o+/-</sub></b>	<b>200 mA / 400 mA</b>
<b>V<sub>clamp</sub></b>	<b>15.6V</b>
<b>Deadtime (typ.)</b>	<b>1.2 <math>\mu</math>s</b>

### Packages



matched to simplify use in 50% duty cycle applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration that operates off a high voltage rail up to 600 volts. In IR2153D a bootstrap diode is included.

### Typical Connections



## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Value		Units
		Min.	Max.	
V <sub>B</sub>	High Side Floating Supply Voltage	-0.3	625	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>LO</sub>	Low Side Output Voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>RT</sub>	R <sub>T</sub> Voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>CT</sub>	C <sub>T</sub> Voltage	-0.3	V <sub>CC</sub> + 0.3	
I <sub>CC</sub>	Supply Current (Note 1)	—	25	mA
I <sub>RT</sub>	R <sub>T</sub> Output Current	-5	5	
dV <sub>S</sub> /dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P <sub>D</sub>	Package Power Dissipation @ T <sub>A</sub> ≤ +25°C (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
R <sub>thJA</sub>	Thermal Resistance, Junction to Ambient (8 Lead DIP)	—	125	°C/W
	(8 Lead SOIC)	—	200	
T <sub>J</sub>	Junction Temperature	—	150	°C
T <sub>S</sub>	Storage Temperature	-55	150	
T <sub>L</sub>	Lead Temperature (Soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Value		Units
		Min.	Max.	
V <sub>B</sub>	High Side Floating Supply Absolute Voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage	—	600	
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>LO</sub>	Low Side Output Voltage	0	V <sub>CC</sub>	
I <sub>CC</sub>	Supply Current (Note 1)	—	5	mA
T <sub>A</sub>	Ambient Temperature	-40	125	°C

Note 1: Because of the IR2153's application specificity toward off-line supply systems, this IC contains a zener clamp structure between the chip V<sub>CC</sub> and COM which has a nominal breakdown voltage of 15.6V. Therefore, the IC supply voltage is normally derived by forcing current into the supply lead (typically by means of a high value resistor connected between the chip V<sub>CC</sub> and the rectified line voltage and a local decoupling capacitor from V<sub>CC</sub> to COM) and allowing the internal zener clamp circuit to determine the nominal supply voltage. Therefore, this circuit should not be driven by a DC, low impedance power source of greater than V<sub>CLAMP</sub>.

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 12V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified.

Symbol	Definition	Value			Units	Test Conditions
		Min.	Typ.	Max.		
$t_r$	Turn-On Rise Time	—	80	—	ns	
$t_f$	Turn-Off Fall Time	—	35	—		
$t_{sd}$	Shutdown Propagation Delay	—	660	—		
DT	Deadtime	—	1.2	—	μs	
D	$R_T$ Duty Cycle	—	50	—	%	

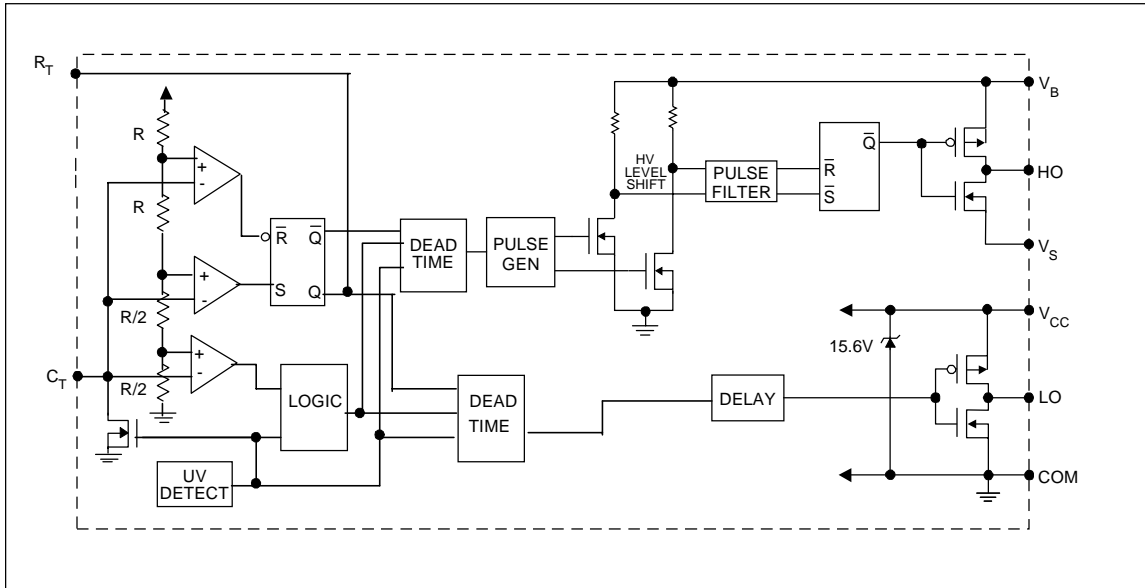
## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 12V,  $C_L$  = 1000 pF,  $C_T$  = 1 nF and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

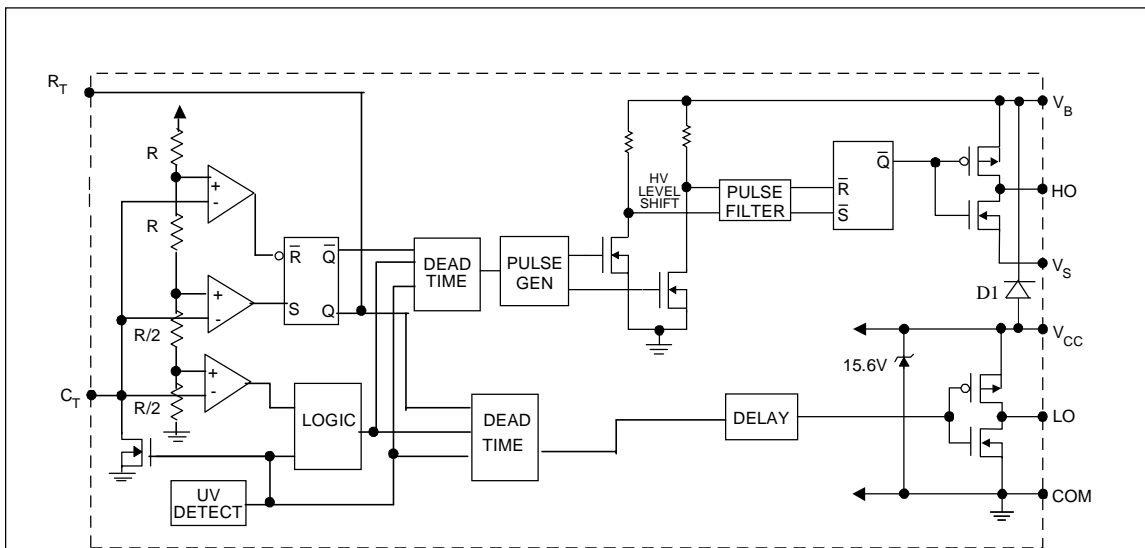
Symbol	Definition	Value			Units	Test Conditions
		Min.	Typ.	Max.		
$f_{OSC}$	Oscillator Frequency	—	20.0	—	kHz	$R_T = 35.7 \text{ k}\Omega$
		—	100	—		$R_T = 7.04 \text{ k}\Omega$
$V_{CLAMP}$	$V_{CC}$ Zener Shunt Clamp Voltage	—	15.6	—	V	$I_{CC} = 5 \text{ mA}$
$V_{CT+}$	2/3 $V_{CC}$ Threshold	—	8.0	—		
$V_{CT-}$	1/3 $V_{CC}$ Threshold	—	4.0	—		
$V_{CTSD}$	$C_T$ shutdown Input Threshold	—	2.2	—		
$V_{RT+}$	$R_T$ High Level Output Voltage, $V_{CC} - R_T$	—	0	100	mV	$I_{RT} = -100 \mu\text{A}$
		—	200	300		$I_{RT} = -1 \text{ mA}$
$V_{RT-}$	$R_T$ Low Level Output Voltage	—	20	50		$I_{RT} = 100 \mu\text{A}$
		—	200	300		$I_{RT} = 1 \text{ mA}$
$V_{OH}$	High Level Output Voltage, $V_{BIAS} - V_O$	—	—	100		$I_O = 0\text{A}$
$V_{OL}$	Low Level Output Voltage, $V_O$	—	—	100		$I_O = 0\text{A}$
$I_{LK}$	Offset Supply Leakage Current	—	—	50	μA	$V_B = V_S = 600\text{V}$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	—	10	—		
$I_{QCCUV}$	Micropower $V_{CC}$ Supply Startup Current	—	90	—		$V_{CC} < V_{CCUV}$
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	—	400	—		$V_{CC} > V_{CCUV}$
$I_{CT}$	$C_T$ Input Current	—	0.001	1.0		
$V_{CCUV+}$	$V_{CC}$ Supply Undervoltage Positive Going Threshold	—	9.0	—	V	
$V_{CCUV-}$	$V_{CC}$ Supply Undervoltage Negative Going Threshold	—	8.0	—		
$V_{CCUVH}$	$V_{CC}$ Supply Undervoltage Lockout Hysteresis	—	1.0	—	V	
$I_{O+}$	Output High Short Circuit Pulsed Current	—	200	—	mA	$V_O = 0\text{V}$
$I_{O-}$	Output Low Short Circuit Pulsed Current	—	400	—		$V_O = 15\text{V}$

# IR2153/IR2153D

## Functional Block Diagram for IR2153



## Functional Block Diagram for IR2153D

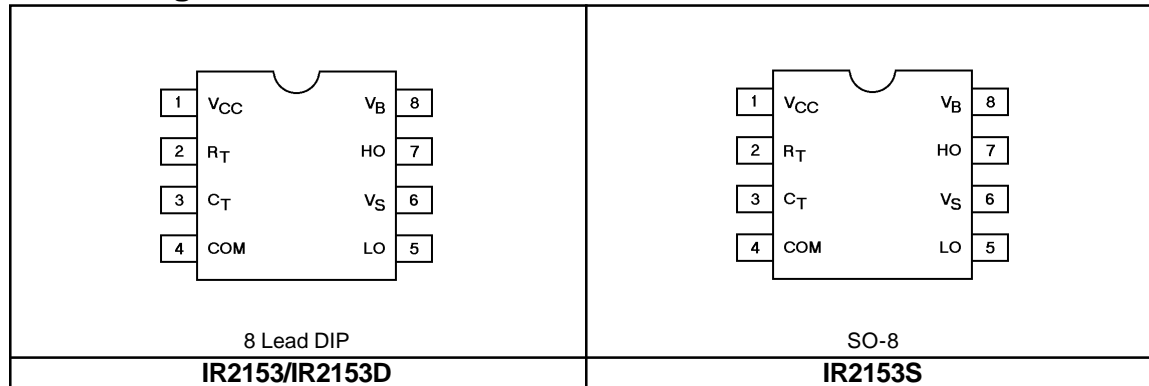


NOTE: The D1 is a separate die.

## Lead Definitions

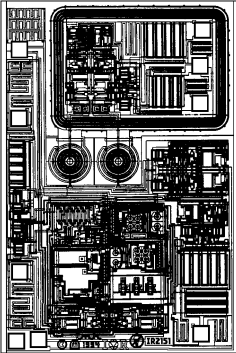
Lead	
Symbol	Description
R <sub>T</sub>	Oscillator timing resistor input, in phase with HO for normal IC operation
C <sub>T</sub>	Oscillator timing capacitor input, the oscillator frequency according to the following equation: $f = \frac{1}{1.4 \times (R_T + 75\Omega) \times C_T}$ where 75Ω is the effective impedance of the R <sub>T</sub> output stage
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return
V <sub>CC</sub>	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

## Lead Assignments



NOTE: The IR2153D is offered in 8 lead DIP only.

## Device Information

Process & Design Rule		HVDCMOS 4.0 $\mu\text{m}$
Transistor Count		231
Die Size		68 X 101 X 26 (mil)
Die Outline		
Thickness of Gate Oxide		800 $\text{\AA}$
Connections	Material	Poly Silicon
	First Layer	Width Spacing Thickness
Second Layer	Material	Al - Si - Cu (Si: 1.0%, Cu: 0.5%)
	Width Spacing Thickness	6 $\mu\text{m}$ 9 $\mu\text{m}$ 20,000 $\text{\AA}$
	Contact Hole Dimension	5 $\mu\text{m}$ X 5 $\mu\text{m}$
Insulation Layer	Material	PSG ( $\text{SiO}_2$ )
	Thickness	1.7 $\mu\text{m}$
Passivation	Material	PSG ( $\text{SiO}_2$ )
	Thickness	1.7 $\mu\text{m}$
Method of Saw		Full Cut
Method of Die Bond		Ablebond 84 - 1
Wire Bond	Method	Thermo Sonic
	Material	Au (1.0 mil / 1.3 mil)
Leadframe	Material	Cu
	Die Area	Ag
	Lead Plating	Pb : Sn (37 : 63)
Package	Types	8 Lead PDIP / SO-8
	Materials	EME6300 / MP150 / MP190
Remarks:		

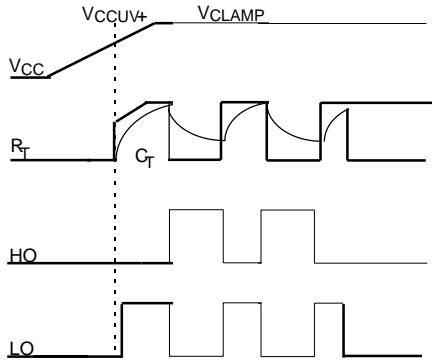


Figure 1. Input/Output Timing Diagram

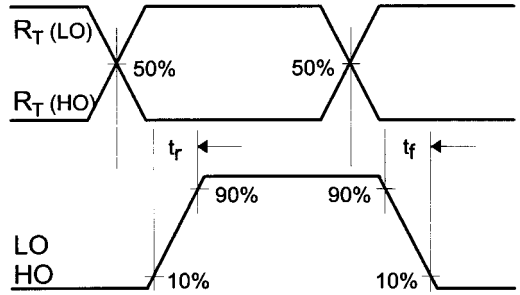


Figure 2. Switching Time Waveform Definitions

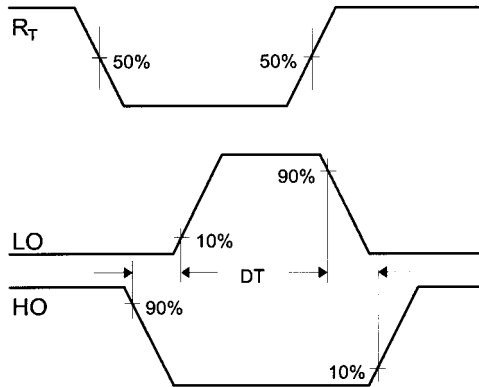
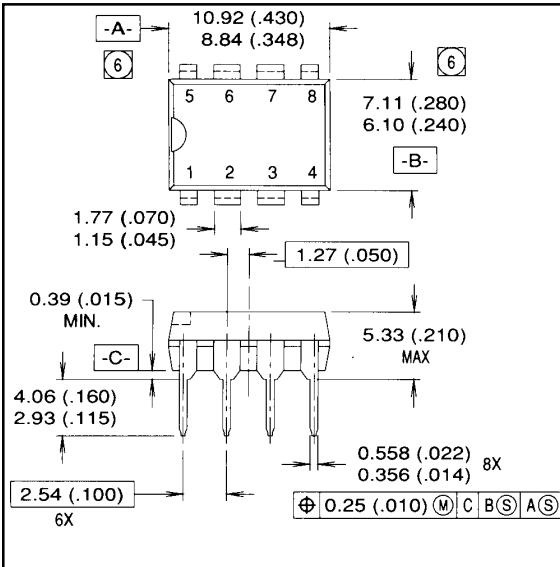
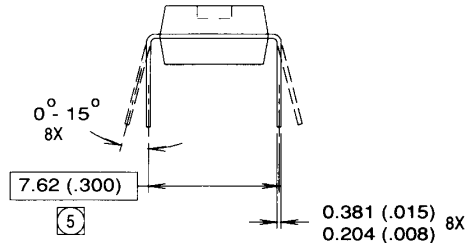


Figure 3. Deadtime Waveform Definitions

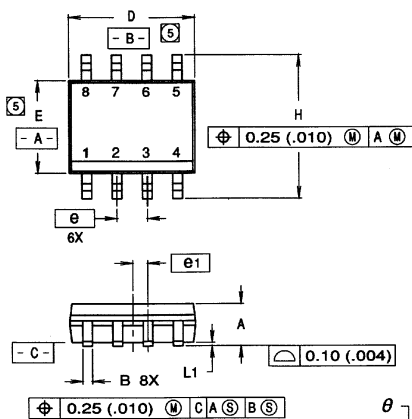


**NOTES:**

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
- 2 CONTROLLING DIMENSION: INCH.
- 3 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
- 5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
- 6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 (.010).



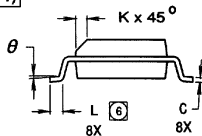
**8 Lead DIP**



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
$\theta$	0°	8°	0°	8°

**NOTES:**

- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
- 2 CONTROLLING DIMENSION: INCH.
- 3 DIMENSIONS DO NOT INCLUDE MOLD FLASH.
- 4 DIMENSIONS SHOWN IN MILLIMETERS (INCHES).
- 5 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.



**SO-8**



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**WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331

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**IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

**IR FAR EAST:** 171 (K&H Bldg.), 30-4 Nishi-ikebukuro 3-Chome, Toshima-ku, Tokyo Japan Tel: 81 3 3983 0086

**IR SOUTHEAST ASIA:** 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

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